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Using Configurable Ultra-Small Clocks to Reduce Space, Power and EMI in Consumer Electronics Designs

Today's tablets and smartphones have more computing power and twice the efficiency of many notebook PCs from a decade ago. Similar trends of increasing performance and size reduction are evident in other handheld consumer products, such as camcorders, digital cameras, media players, GPS systems and personal gaming consoles. Given this consumer electronics market dynamic, if the portable device doesn't fit in your pocket, it will soon become outdated. In fact, it seems as soon as we get comfortable with a new consumer electronic gadget, a lighter, smaller, greener, more powerful version appears on the market. Semiconductor components play a major role in this evolution to ultra-small form factors, and timing devices are no exception in this market trend.

Every digital electronic system requires a repetitive periodic signal or frequency that sets the timing for all data transactions within the system and with interface devices. Silicon timing devices have gone through an evolution that impacts not only frequency generation but also board space occupation, power consumption, electromagnetic interference (EMI), and the flexibility of configuration to adapt to rapid changes in design cycles. Let's explore the implications of these latest timing device trends as well as the benefits of using configurable silicon timing devices to address ever-evolving system requirements.

Saving Space with Ultra-Small Clocks

Space constraints are a major concern for system board designers focused on consumer products. Any possible reduction in used printed circuit board (PCB) space allows more room for routing signals, bypassing noise on power supplies, or simply reducing PCB cost. Numerous timing device vendors support small-outline clock generators optimized for the consumer electronics industry. Although very critical for system operation, the clock generator is generally not considered a key component on the board; therefore, it is occasionally overlooked when it comes to space savings. If that is the case, the embedded designer should reconsider the options and realize the significant space savings that a silicon clock generator can offer.

Consider a digital camera that requires three crystals or oscillators in the system to provide the necessary clocking for a USB controller operating at 24 MHz, for the high-speed analog-to-digital convertor (ADC) (also at 24 MHz) and for the image processor at 27 MHz. Although it carries a higher cost than other larger crystals, the popular small surface-mount crystal has a standard size of 2 mm x 1.6 mm. This crystal runs fundamental frequencies typically ranging from 24 MHz to 54 MHz and is packaged in a ceramic housing available from many major industry suppliers.

If one or two of these three crystals were replaced by a Silicon Labs Si51210 clock generator with an ultra-small 1.4 mm x 1.2 mm package size, the digital camera designer would be able to reduce the system's clock space usage by a considerable 47 to 73 percent. CMOS-based clock generators are mixed-signal semiconductor devices that employ a phase-locked loop (PLL) architecture typically used to generate output frequencies that are different from the input. If the device is configurable, the designer will be able to generate any frequency that best fits the system requirements.

Minimizing Power Consumption

System designers have many choices to make when it comes to selecting a clock generator. Since market trends favor greener, more power-efficient systems, it is important to consider certain factors impacting power consumption when making the clock selection. Understanding the silicon gate geometry, the core power supply and the ability to configure output drive are key factors in determining how “low-power-friendly” a clock generator will be. Power consumption in CMOS depends on the switching speed, the power supply level, and the load capacitance that the device is driving based on the following formula: $P = C_L * V^2 * F$

C_L is a representation of the load capacitance, which is relative to the gate size and thus dependent on the submicron CMOS technology being implemented. Making the device affordable at a smaller gate width technology, such as 0.18 micron, is critical. The device’s ability to support a lower supply voltage (V) has an exponential impact on power consumption as can be seen in the above formula. It is important, however, to consider the availability of the power supply in the system. For example, 1.8 V is a widely-used power supply across multiple handheld and AC-powered applications.

In addition to these power-related parameters, device configurability plays a significant role when considering power consumption minimization. In the case of the Si51210 clock, the device allows different output drive strength levels to accommodate different types of loading and trace lengths, allowing the designer to minimize the overshoot and undershoot of the clock. Referencing the formula $I = C dv/dt$, it is noticeable that keeping dv at its minimum is ideal for minimizing current consumption. In the case of clock output signals: $dv = V_{out_max}$ (maximum output swing level) – VDD (power supply voltage). Therefore, it is advantageous to keep V_{out_max} as close as possible to VDD.

Reducing EMI

EMI reduction remains an important consideration when bringing electronic systems to market. Regardless of the system’s performance, features and other innovations, if the system cannot pass government regulations for electromagnetic emissions, the manufacturer may not be able to launch the product. This barrier to production heavily burdens system designers as well as EMI compliance engineers. In particular, the emission compliance test takes place after the board has been designed and just as the system is reaching the last phase of pre-production. Therefore, it is important to address EMI issues during the design stage or risk delays in launching the product to the market. This is no easy task considering that unpredictable real-life noise models may be difficult to identify during board simulation. Conventional techniques for EMI reduction including shielding and localized filtering are relatively simple but can be costly. In most systems today, especially for portable and handheld products, shielding becomes the least desirable method of EMI reduction due to size, weight and manufacturing cost.

To reduce the need to place passive components across the board to control potential noise and EMI behavior, the designer should consider choosing a clock generator that integrates a frequency modulation technique referred to as spread spectrum or spectrum spread. As the name suggests, spread spectrum technology distributes the energy that is typically concentrated at the center frequency over a wider bandwidth, consequently attenuating the peak energy.

Figure 1 shows the spectral energy of a clock running at 38.4 MHz with and without spread spectrum as measured on a spectrum analyzer. The difference in peak energy is visible and measurable in the EMI chamber. Using this modulation technique, the higher the frequency, the more attenuation is visible, effectively achieving higher dB reduction at the harmonics where it really matters.

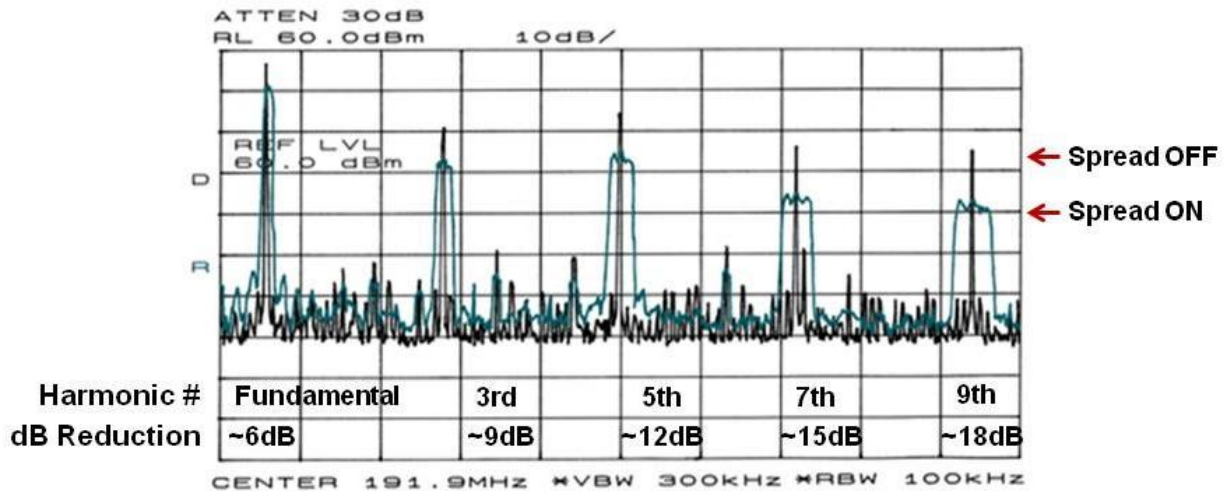


Figure 1. Spectral Energy of Clock Running at 38.4 MHz

The configurable clock generator supports various configurable settings of the spread bandwidth and gives the EMI engineer more options for optimizing the system setting.

In addition, the ability to change rise and fall times of the clock allows additional attenuation of the EMI generated by the clock itself. Consider the Fourier transform of a square wave:

$$f(x) = \frac{4}{\pi} \left(\sin 2\pi f x + \frac{1}{3} \sin 6\pi f x + \frac{1}{5} \sin 10\pi f x + \frac{1}{7} \sin 14\pi f x + \dots \right)$$

When the rise and fall times are slower, the clock's waveform deviates from a square wave, hence attenuating the odd harmonics gain.

Configurability Benefits

Using the signal integrity tuning features of an advanced configurable clock generator, the designer can reduce the budgeted amount of several of these timing errors. In addition, confidence in a sufficient timing margin can be increased by artificially introducing errors to validate the error modeling. For example, the highly programmable Si51210 clock generator enables fine-tuning of the output drive strength, operating frequency, spread spectrum profile and modulation rate to minimize timing errors and validate the amount of time needed for the system timing margin. These programmable features can also be used to determine system response to intentional timing errors. This is a very useful debugging tool during development to measure the system's sensitivity to various timing parameters.

Programming the clock to set all timing error deltas (Tr/Tf, period, spread spectrum magnitude, etc.) to the maximum allowed by specification and then running the system to the point of failure can prove the actual frequency limit. Of course, some small margin is still retained for safety, and the timing specifications of the other components remain unaffected.

Ultimately, the advantages of configurability allow the designer to adapt to any changes in frequency or drive requirements of the receiver devices even in if the changes occur in the middle of the design cycle. In addition, the ability to quickly reconfigure frequency, drive levels and spread spectrum parameters while maintaining the same device pinout enables the designer to port the layout to the next project, thereby reducing the development time for the timing system.